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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/637,663	08/11/2003	Wataru Itoh	60188-632	3512

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EXAMINER	
RADOSEVICH, STEVEN D	

ART UNIT	PAPER NUMBER
2138	

DATE MAILED: 12/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/637,663	ITOH ET AL.	
	Examiner	Art Unit	
	Steven D. Radosevich	2138	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 August 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☐ Claim(s) _____ is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08/11/2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

1. Claims 1-7 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

2. Claims 1 recites the limitation "the application environment" in line 6. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-13 rejected under 35 U.S.C. 102(b) as being anticipated by Fukuda (US 2001/0054166 A1).

4. As per claim 1: Fukuda teaches an assembly for an LSI test which supplies a test signal output (108 - paragraph 7 line 4) from an LSI tester (12 - paragraph 6 line 5) to a target LSI (20; figure 1, paragraph 6 line 5) to be tested and outputs, to the LSI tester (12 - paragraph 6 line 5), a test result signal (104-paragraph 7 Line 9) generated by processing of the target LSI (20; figure 1, paragraph 6 line 5) performed in accordance with the test signal (108 - paragraph 7 line 4), the assembly comprising:

A peripheral circuit (BIST circuit or Logic circuit or PLL circuit - paragraph 6 line 3, or IC tester- paragraph 6 line 2) coupled to the target LSI (20; figure 1, paragraph 6 line 5) and allowing the target LSI (20; figure 1, paragraph 6 line 5) to operate in the same manner as in the application environment; and

A printed circuit board (15 or 14 or 13 or 12 - paragraph 6 lines 3-5, figure 1) on which the peripheral circuit (BIST circuit or Logic circuit or PLL circuit - paragraph 6 line 3, or IC tester - respectively - paragraph 6 line 2) is mounted.

5. As per claim 2: Fukuda teaches the above assembly for an LSI test including:

A first board (10 - figure 3) including the peripheral circuit (Logic circuit or PLL circuit - paragraph 6 line 3) and the printed circuit board (14 or 13 - paragraph 6 line 3, figure 1); and

A second board (15 - figure 3) coupled to the first board (10 - figure 3) and including wiring (see figure 1, 3, and 5) for coupling the first board (10 - figure 3) and the LSI tester (12 - paragraph 6 line 5) to each other.

6. As per claim 3: Fukuda teaches the above assembly for an LSI test wherein the test signal (108 - paragraph 7 line 4) is supplied to the peripheral circuit (BIST – figure 1) and then output (paragraph 7 line 4) from the peripheral circuit (BIST – figure 1) to the target LSI (20; figure 1, paragraph 6 line 5).

7. As per claim 4: Fukuda teaches the above assembly for an LSI test wherein the test result signal (104 – paragraph 7 line 9, figure 1) is supplied to the peripheral circuit (BIST – figure 1, paragraph 7 line 9) and then output (107 – paragraph 7 line 16) from the peripheral circuit (BIST – figure 1) to the LSI tester (12 - paragraph 7 lines 13-14).

8. As per claim 5: Fukuda teaches the above assembly for an LSI test wherein a memory (BIST circuit - paragraph 7 line 9-11, IC tester - paragraph 7 lines 17-19) is provided as the peripheral circuit or in the target LSI, and the LSI tester (12 - paragraph 6 lines 13-14) is configured to be capable of accessing the memory asynchronously to a clock supplied (paragraph 7 lines 16-17) to the target LSI (12 - paragraph 7 lines 16-17)

9. As per claim 6: Fukuda teaches the above assembly for an LSI test wherein the test signal (108 - paragraph 7 line 4) is stored in the memory (BIST circuit – paragraph 7 line 9-11/figure 1, IC tester paragraph 7 line 17-18), and then read out (paragraph 7 line 3-4) from the memory to be processed by the target LSI (20; figure 1, paragraph 6 line 5).

10. As per claim 7: Fukuda teaches the above assembly for an LSI test wherein the test result signal (104 - paragraph 7 line 10) is stored in the memory (paragraph 7 line 12), and then read out from the memory (paragraph 7 lines 12-16) to the LSI tester (12 - paragraph 7 lines 17-18).

11. As per claim 8: Fukuda teaches an assembly for an LSI test which supplies a test signal (108 - paragraph 7 line 4) output from an LSI tester (12 - paragraph 7 line 3) to a target LSI (20 – paragraph 7 line 4) to be tested an outputs, to the LSI tester (12 - paragraph 7 line 3), a test result signal (107 – paragraph 7 line 16) generated by processing of the target LSI (20 – paragraph 7 line 4) performed in accordance with the test signal (108 - paragraph 7 line 4), the assembly comprising:

A test result receiving circuit (BIST circuit – paragraph 7 line 9) for performing given processing on data (104 – paragraph 7 line 9) obtained as the

result signal (107 – paragraph 7 line 16) so as to reduce (compresses – paragraph 7 line 10) the amount of the data (104 – paragraph 7 line 9), and for outputting a result (107 – paragraph 7 line 16) of the processing to the LSI tester (12 - paragraph 7 lines 17-18), and

A printed circuit board (15 – paragraph 7 line 9, figure 1) on which the test result receiving circuit (BIST circuit – paragraph 7 line 9) is mounted.

12. As per claim 9: Fukuda teaches the above assembly for an LSI test wherein an enable control circuit (BIST – paragraph 7 line 9) for selecting necessary data (compresses – paragraph 7 line 10) from the data obtained as the test result signal (104 – paragraph 7 line 9) and for outputting the selected data (107 – paragraph 7 line 16) is provided in the test result receiving circuit (BIST circuit – paragraph 7 line 9) of in the target LSI (20 – paragraph 7 line 4).

13. As per claim 10: Fukuda teaches the above assembly for an LSI test wherein the test result receiving circuit (BIST – paragraph 7 line 9) includes a compression circuit (paragraph 7 line 10) for compressing input data (104 – paragraph 7 line 9) and outputting the compressed data (107 – paragraph 7 line 16).

14. As per claim 11: Fukuda teaches the above assembly for an LSI test wherein the test result receiving circuit (BIST – paragraph 7 line 9) includes a determination circuit (PLL circuit – paragraph 8 line 2) for determining (paragraph 8 line 3) whether or not the input data (paragraph 8 line 3) coincides with data to be input (paragraph 8 line 4) when the target LSI operates normally, and outputting a result of the determination (paragraph 8 lines 9-11).

15. As per claim 12: Fukuda teaches an LSI test system, comprising:

An LSI tester (12 IC tester – paragraph 7 lines 2-3) for supplying a test signal (108 – paragraph 7 lines 3-4) to a target LSI (LSI 20 – paragraph 7 line 4) to be tested; and

An assembly for an LSI test which outputs, to the LSI tester (12 IC tester – paragraph 7 lines 2-3), a result signal (107 – paragraph 7 line 16) generated by processing of the target LSI (LSI 20 – paragraph 7 line 4) performed in accordance with the test signal (108 – paragraph 7 lines 3-4), wherein the assembly comprises:

A peripheral circuit (BIST circuit – paragraph 7 line 9) coupled to the target LSI (LSI 20 – paragraph 7 line 4) and allowing the target LSI (LSI 20 – paragraph 7 line 4) to operate in the same manner as in the application environment; and

A printed circuit board (15 – figure 1) on which the peripheral circuit (BIST circuit – paragraph 7 line 9) is mounted.

16. As per claim 13: Fukuda teaches an LSI test method, comprising the steps of:

Operating a non-defective LSI (LSI 20 – paragraph 7 line 4), which is configured as a target LSI (LSI 20 – paragraph 7 line 4) to be tested and has been confirmed (paragraph 8 lines 9-11) to operate normally, in a circuit equivalent to a circuit actually used (paragraph 8 line 10), and generating and storing a test signal and a reference test result signal (paragraph 7 lines 9-10, 17-20), based on a signal supplied (108 – paragraph 7 lines 3-4) to the non-

defective LSI (LSI 20 – paragraph 7 line 4) and a signal output (107 – paragraph 7 line 16) from the non-defective LSI (LSI 20 – paragraph 7 line 4), respectively; and

Supplying the test signal (108 – paragraph 7 lines 3-4) to the target LSI (LSI 20 – paragraph 7 line 4) to compare (paragraph 7 line 18) a test result signal (107 – paragraph 7 line 18) generated by the target LSI (LSI 20 – paragraph 7 line 4) in accordance with the test signal (108 – paragraph 7 lines 3-4), with the reference test result signal (expected data – paragraph 7 line 19), thereby determining whether or not the target LSI (LSI 20 – paragraph 7 line 4) is defective (paragraph 7 line 19).Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven D. Radosevich whose telephone number is 571-272-2745. The examiner can normally be reached on 9am-5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on 571-272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Steven D. Radosevich
Examiner
Art Unit 2138

SUPERVISORY PATENT EXAMINER